

CLAIMS

Having thus described our invention in detail, what we claim is new and desire to secure by the Letters Patent is:

- 1 1. A method of forming a metal-insulator-silicon (MIS) capacitor comprising the
2 steps of:
3
4 (a) implanting a bottom electrode into a surface of a Si-containing substrate;
5
6 (b) forming a high-k dielectric over at least a portion of said bottom electrode, said
7 high-k dielectric having a dielectric constant of greater than about 8.0; and
8
9 (c) forming a doped Si-containing electrode over said high-k dielectric, wherein said
10 doped Si-containing electrode comprises an intrinsic base polysilicon layer of a
11 bipolar device.
- 1 2. The method of Claim 1 wherein step (a) includes a high-dose reach-thru implant
2 which provides a doped region having a dopant concentration of about $1E19$
3 atoms/cm³ or above
- 1 3. The method of Claim 1 wherein following said implant step said bottom electrode
2 is annealed in an inert gas.
- 1 4. The method of Claim 1 wherein said high-k dielectric is formed by a deposition
2 process selected from the group consisting of low pressure chemical vapor deposition,
3 atomic layer chemical vapor deposition, rapid thermal chemical vapor deposition,
4 plasma-assisted chemical vapor deposition, physical vapor deposition, sputtering,
5 plating, evaporation and chemical solution deposition.
- 1 5. The method of Claim 1 wherein said high-k dielectric is a binary metal oxide, a
2 silicate, aluminate, or oxynitride of a binary metal oxide, or a perovskite oxide.

- 1 6. The method of Claim 5 wherein said high-k dielectric is a binary metal oxide or an
2 aluminate of a binary metal oxide.
- 1 7. The method of Claim 6 wherein said high-k dielectric is Al_2O_3 .
- 1 8. The method of Claim 1 wherein said high-k dielectric has a thickness of from about
2 50 to about 1000 Å.
- 1 9. The method of Claim 1 wherein a diffusion barrier layer is formed on said bottom
2 electrode prior to formation of said high-k dielectric, on said high-k dielectric or both.
- 1 10. The method of Claim 1 wherein said high-k dielectric and said doped Si-
2 containing electrode are patterned after performing step (c).
- 1 11. The method of Claim 10 wherein said patterning includes lithography and etching.
- 1 12. The method of Claim 1 wherein said doped Si-containing electrode comprises
2 poly SiGe.
- 1 13. The method of Claim 1 wherein said doped Si-containing electrode is formed by
2 deposition and ion implantation or by an in-situ doping deposition process.
- 1 14. The method of Claim 10 wherein spacers are formed on exposed sidewalls of said
2 patterned high-k dielectric and said patterned doped Si-containing electrode.
- 1 15. The method of Claim 11 wherein an amorphization step follows said lithography
2 step.
- 1 16. A MIS capacitor integrated with a bipolar device comprising an implanted bottom
2 electrode formed in a surface of a Si-containing substrate; a high-k dielectric having a

3 dielectric constant of greater than about 8 formed on a portion of said implanted
4 bottom electrode; and a doped Si-containing electrode formed on said high-k
5 dielectric, wherein said doped Si-containing electrode comprises an intrinsic base
6 polysilicon layer of a bipolar device.

1 17. The MIS capacitor of Claim 16 wherein said high-k dielectric is a binary metal
2 oxide, a silicate, aluminate or oxynitride of a binary metal oxide, or a perovskite
3 oxide.

1 18. The MIS capacitor of Claim 17 wherein said high-k dielectric is a binary metal
2 oxide or an aluminate of a binary metal oxide.

1 19. The MIS capacitor of Claim 18 wherein said high-k dielectric is Al_2O_3 .

1 20. The MIS capacitor of Claim 16 wherein said doped Si-containing electrode is
2 composed of poly SiGe.

1 21. The MIS capacitor of Claim 16 wherein spacers are present on any exposed
2 sidewalls of said high-k dielectric and said doped Si-containing electrode.

1 22. The MIS capacitor of Claim 16 wherein a diffusion barrier layer is present
2 between said bottom electrode and said high-k dielectric, between said high-k
3 dielectric and said doped Si-containing electrode, or between said bottom electrode
4 and said high-k dielectric and between said high-k dielectric and said doped Si-
5 containing electrode.

1 23. A method of fabricating a poly-poly capacitor comprising the steps of:

2

3 (a) forming a base polysilicon layer over at least isolation regions;

4

5 (b) forming a high-k dielectric over at least a portion of isolation regions, wherein said
6 high-k dielectric has a dielectric constant of greater than about 8.0; and
7
8 (c) forming a doped Si-containing electrode over said high-k dielectric, wherein said
9 doped Si-containing electrode comprises an intrinsic base polysilicon layer of a
10 bipolar device.

1 24. The method of Claim 23 wherein said isolation regions are local oxidation of
2 silicon regions or trench isolation regions.

1 25. The method of Claim 23 wherein said base polysilicon layer is formed by a
2 deposition process selected from the group consisting of chemical vapor deposition,
3 plasma-assisted chemical vapor deposition, sputtering evaporation, and chemical
4 solution deposition.

1 26. The method of Claim 23 wherein said base polysilicon layer is doped by ion
2 implantation.

1 27. The method of Claim 23 wherein said base polysilicon layer is comprised of poly
2 SiGe.

1 28. The method of Claim 23 wherein said high-k dielectric is formed by a deposition
2 process selected from the group consisting of low pressure chemical vapor deposition,
3 atomic layer chemical vapor deposition, rapid thermal chemical vapor deposition,
4 plasma-assisted chemical vapor deposition, physical vapor deposition, sputtering,
5 plating, evaporation and chemical solution deposition.

1 29. The method of Claim 23 wherein said high-k dielectric is a binary metal oxide, a
2 silicate, aluminate or oxynitride of a binary metal oxide, or a perovskite oxide.

- 1 30. The method of Claim 29 wherein said high-k dielectric is a binary metal oxide or
2 an aluminate of a binary metal oxide.
- 1 31. The method of Claim 30 wherein said high-k dielectric is Al_2O_3 .
- 1 32. The method of Claim 23 wherein said high-k dielectric has a thickness of from
2 about 50 to about 1000 Å.
- 1 33. The method of Claim 23 wherein a diffusion barrier layer is formed on said
2 bottom electrode prior to formation of said high-k dielectric, on said high-k dielectric
3 or both.
- 1 34. The method of Claim 23 wherein said high-k dielectric and said doped Si-
2 containing electrode are patterned after performing step (c).
- 1 35. The method of Claim 34 wherein said patterning includes lithography and etching.
- 1 36. The method of Claim 23 wherein said doped Si-containing electrode comprises
2 poly SiGe.
- 1 37. The method of Claim 23 wherein said doped Si-containing electrode is formed by
2 deposition and ion implantation or by an in-situ doping deposition process.
- 1 38. The method of Claim 34 wherein spacers are formed on exposed sidewalls of said
2 patterned high-k dielectric and said patterned doped Si-containing electrode.
- 1 39. The method of Claim 35 wherein an amorphization step follows said lithography
2 step.
- 1 40. A poly-poly capacitor comprising a bottom polysilicon electrode formed over
2 isolation regions that are present in a Si-containing substrate; a high-k dielectric

3 having a dielectric constant of greater than about 8 formed on a portion of said bottom
4 electrode; and a doped Si-containing electrode formed on said high-k dielectric,
5 wherein said doped Si-containing electrode comprises an intrinsic base polysilicon
6 layer of a bipolar device.

1 41. The poly-poly capacitor of Claim 40 wherein said bottom polysilicon electrode is
2 composed of poly SiGe.

1 42. The poly-poly capacitor of Claim 40 wherein said high-k dielectric is a binary
2 metal oxide, a silicate, aluminate or oxynitride of a binary metal oxide, or a perovskite
3 oxide.

1 43. The poly-poly capacitor of Claim 42 wherein said high-k dielectric is a binary
2 metal oxide or an aluminate of a binary metal oxide.

1 44. The poly-poly capacitor of Claim 43 wherein said high-k dielectric is Al_2O_3 .

1 45. The poly-poly capacitor of Claim 40 wherein said doped Si-containing electrode
2 is comprised of poly SiGe.

1 46. The poly-poly capacitor of Claim 40 wherein spacers are present on any exposed
2 sidewalls of said high-k dielectric and said doped Si-containing electrode.

1 47. The poly-poly capacitor of Claim 40 wherein a diffusion barrier layer is present
2 between said bottom electrode and said high-k dielectric, between said high-k
3 dielectric and said doped Si-containing electrode, or between said bottom electrode
4 and said high-k dielectric and between said high-k dielectric and said doped Si-
5 containing electrode.